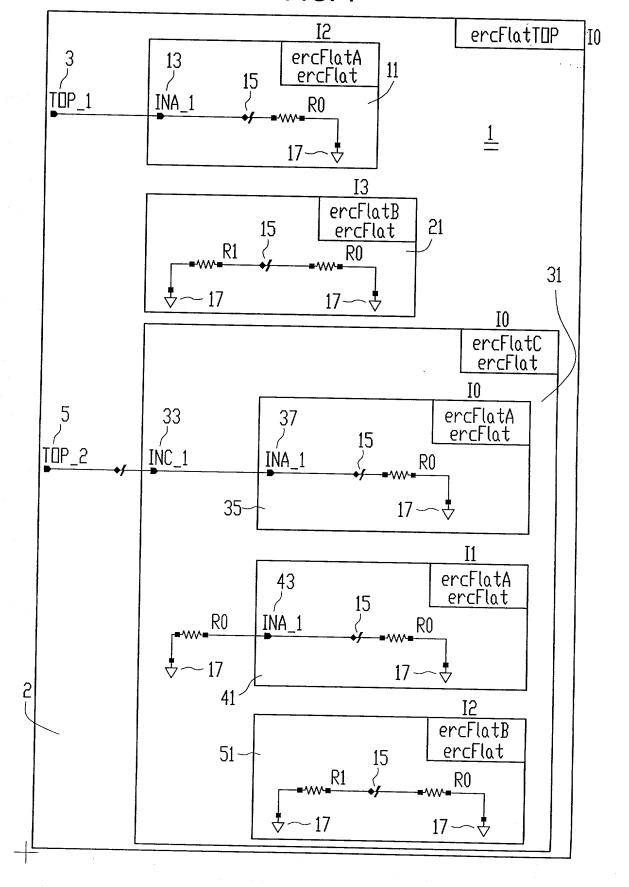
FIG. 1



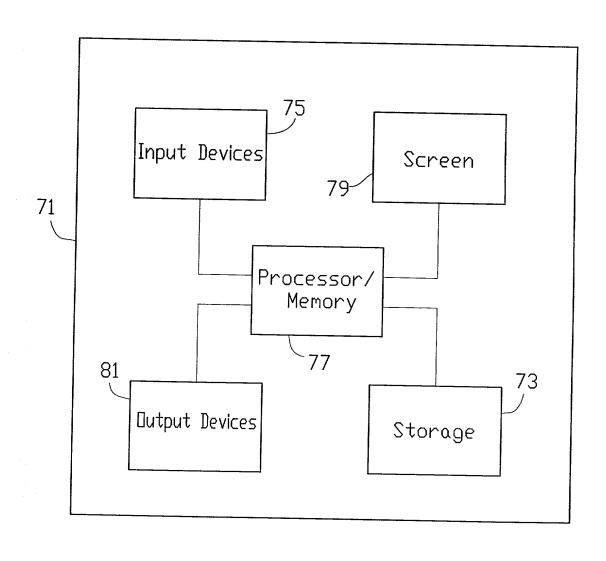


FIG. 3

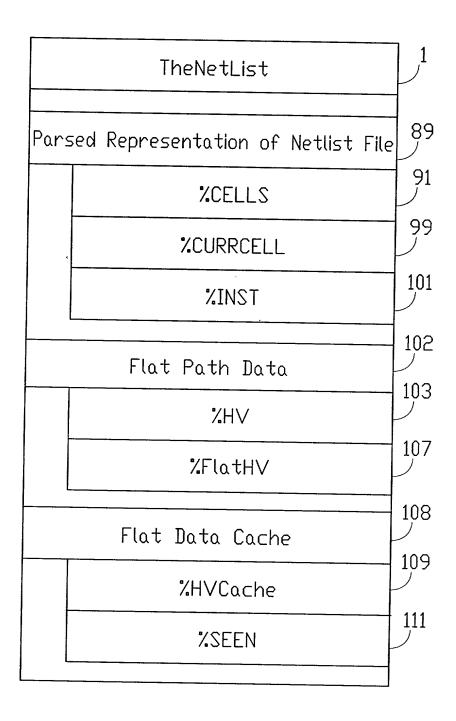
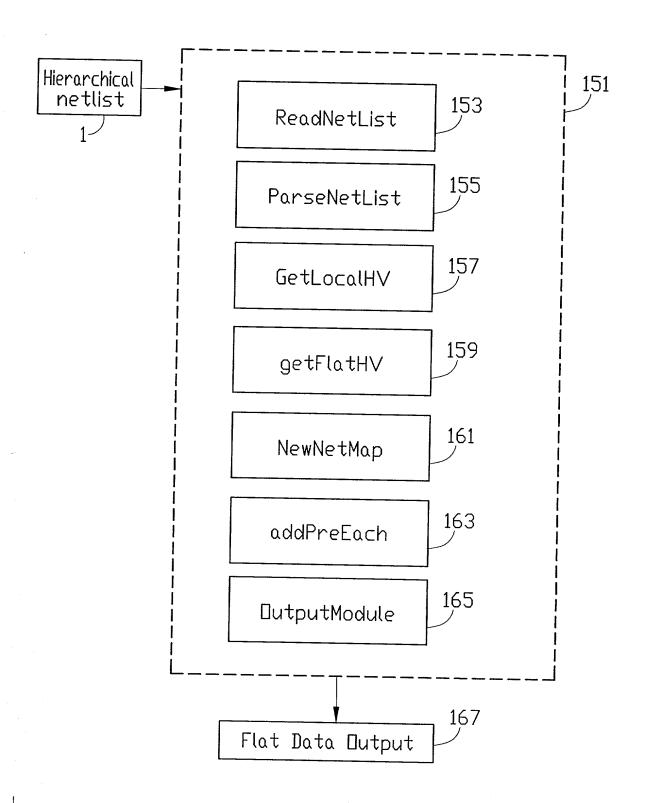


FIG. 4



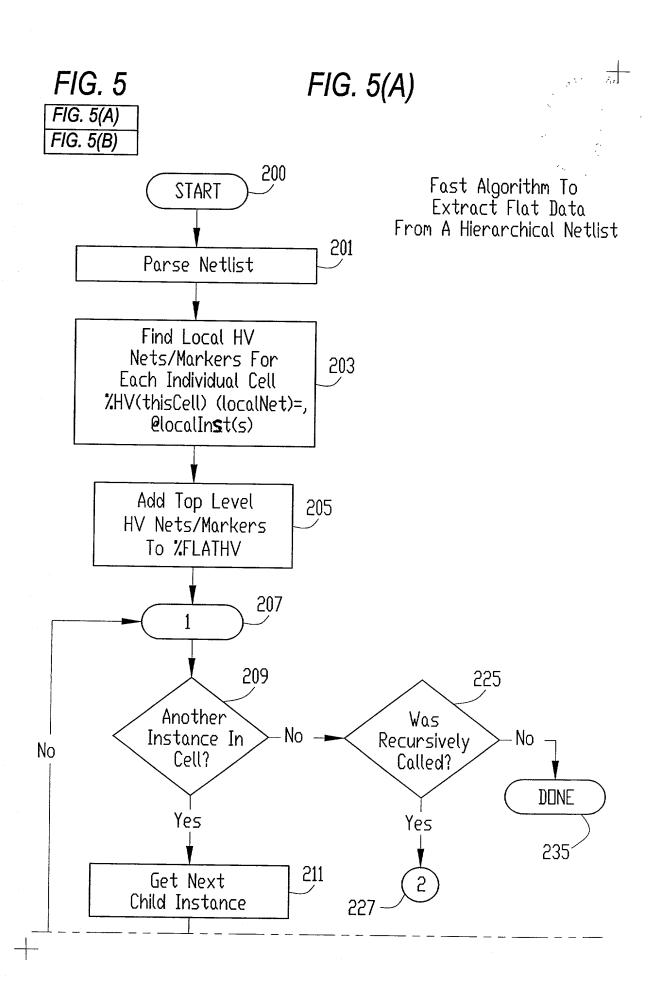
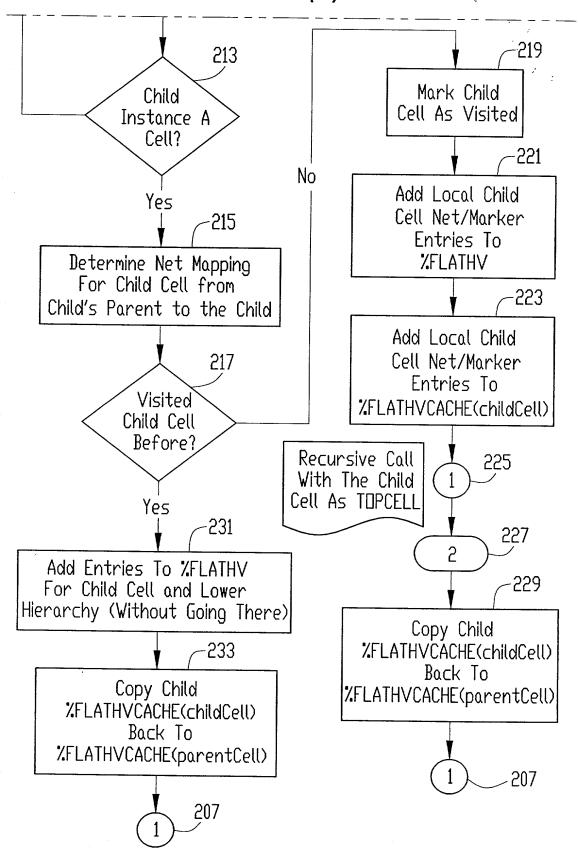


FIG. 5(B)



## FIG. 6(B)

```
Flat
    INA_1---->( X0 )
  Check
  Deep
Cell=<ercFlatB>
  Flat
  Check
  Deep
    net2---->(X0)
Cell=<ercFlatTOP>
  Flat
  Check
    TOP_1---->( I2/X0 )
    TOP_2--->( IO/IO/XO )
                                           305
  Deep
    I0/net2---->( I0/I1/X0 )
    I0/I2/net2---->( I0/I2/X0 )
    I3/net2----> (I3/X0)
Cell=(ercFlatC)
  Flat
  Check
    net2---->( I1/X0 )
    INC_1---->( IO/XO )
  Deep
    I2/net2---->( I2/X0 )
```

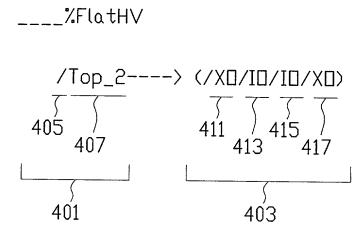
FIG. 6(A) FIG. 6(B)

FIG. 6(A)

## PROGRAM OUTPUT

```
-----%HV...
       inst=<ercFlatA>
          \langle INA_1 \rangle ---->(\langle X0 \rangle)
       inst=<ercFlatB>
                                                     301
          \langle net2 \rangle ----- \rangle (\langle X0 \rangle)
       inst=<ercFlatTOP>
          (T□P_2> ---->( ⟨X0> )
                 -----%FLATHV...
       /I0/net2---->( /I0/I1/X0 )
top
       /TOP_1---->( /I2/X0 )
path
       /I0/I2/net2---->( /I0/I2/X0 )
keys
       /I3/net2---->(/I3/X0)
                                                         303
       /TOP_2---->( /X0 /I0/I0/X0 )
                    ----%FLATHVCACHE...
       Cell=<ercFlatA>
```

FIG. 7



1